

Universal Asynchronous Receiver/Transmitter UART

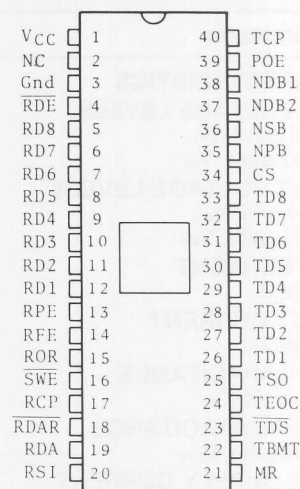
FEATURES

- ☐ Low Power — 10mw @ 3.2MHz typical
- ☐ Single +5v power supply
- ☐ DC to 3.2MHz
- ☐ TTL Compatible
- ☐ Full or Half Duplex Operation — can receive and transmit simultaneously at different baud rates
- ☐ Fully Double Buffered — eliminates need for precise external timing
- ☐ Start Bit Verification — decreases error rate
- ☐ Fully Programmable — data word length, parity mode, number of stop bits; one, one and one-half, or two
- ☐ Tri-State Outputs — bus structure oriented
- ☐ Baud Rate Clock Generated by COM 8046
- ☐ Hermetic DIP Package — easy board insertion
- ☐ Pin for pin replacement for: Harris HD-6402, Intersil IM6402
- ☐ Compatible with Industry Standard UARTs

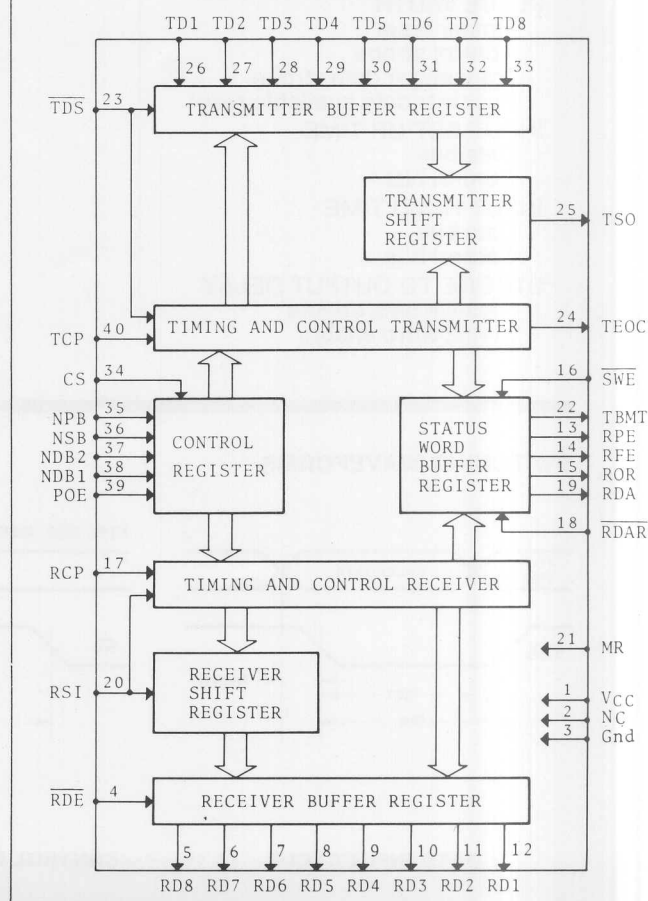
General Description

The Universal Asynchronous Receiver/Transmitter is a CMOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with asynchronous data communications and processor interfacing. CMOS/LSI technology permits operating clock frequencies up to 3.2MHz (200K Baud) while requiring only 10mw of power. The duplex mode, baud rate, data word length, parity mode, and number of stop bits are independently programmable through the use of external controls. There may be 5, 6, 7, or 8 data bits, odd/even or no parity, and 1, or 2 stop bits or 1.5 stop bits when utilizing a 5-bit code. These programmable features provide the user with the ability to interface with a wide range of peripherals, modems, and remote data acquisition systems.

Pin Configuration



Functional Block Diagram



MAXIMUM GUARANTEED RATINGS*

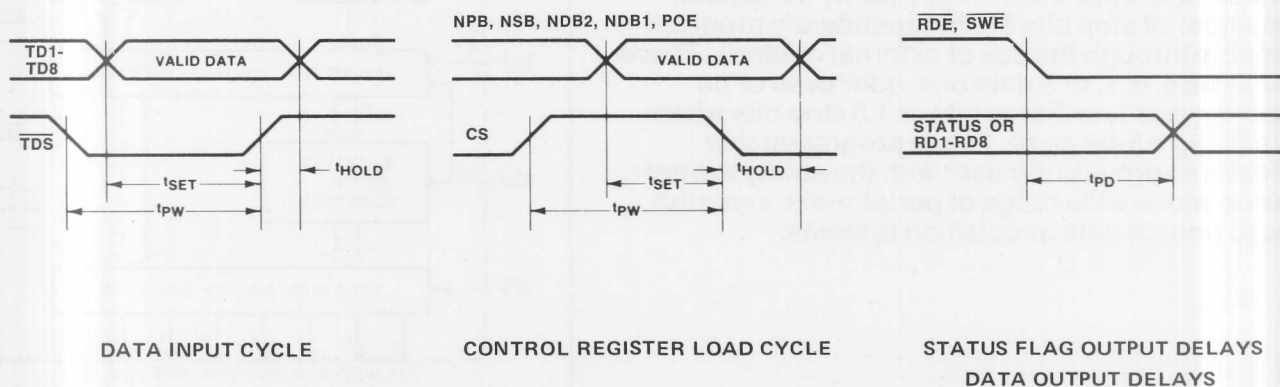
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin	V _{CC} +0.3V
Negative Voltage on any Pin	GND -0.3V
Supply Voltage	+8V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-Level, V _{IL}			0.8	V	
High-Level, V _{IH}	V _{CC} -2.0		V _{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V _{OL}		0.2	0.4	V	I _{OL} = 1.6mA
High-Level, V _{OH}	2.4	4.0		V	I _{OH} = 200μA
INPUT CURRENT					
Leakage, I _I	-1.0		1.0	μA	0 ≤ V _{IN} ≤ +5V
OUTPUT CURRENT					
Leakage, I _O			-1	μA	$\overline{SWE} = \overline{RDE} = V_{IH}, 0 \leq V_{OUT} \leq +5V$
INPUT CAPACITANCE					
All inputs, C _{IN}		5	10	pf	V _{IN} = V _{CC} , f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C _{OUT}		5	10	pf	$\overline{SWE} = \overline{RDE} = V_{IH}, f = 1MHz$
POWER SUPPLY CURRENT					
I _{CC}		1.0	100	μA	All outputs = V _{OH} T _A = +25°C, V _{CC} = +5V
A.C. CHARACTERISTICS					
CLOCK FREQUENCY					
RCP, TCP	DC		3.2	MHz	
PULSE WIDTH					
Master reset		500		ns	MR
Control strobe		200		ns	CS
Transmitter data strobe		200		ns	TDS
Receiver data available reset		200		ns	RDAR
INPUT SET-UP TIME					
Data bits		100		ns	TD1-TD8
Control bits		100		ns	NPB, NSB, NDB2, NDB1, POE
INPUT HOLD TIME					
Data bits		100		ns	TD1-TD8
Control bits		100		ns	NPB, NSB, NDB2, NDB1, POE
STROBE TO OUTPUT DELAY					
Receive data enable		200	350	ns	Load = 20pf + 1 TTL input RDE: T _{PD1} , T _{PDO}
Status word enable		200	350	ns	SWE: T _{PD1} , T _{PDO}

SWITCHING WAVEFORMS



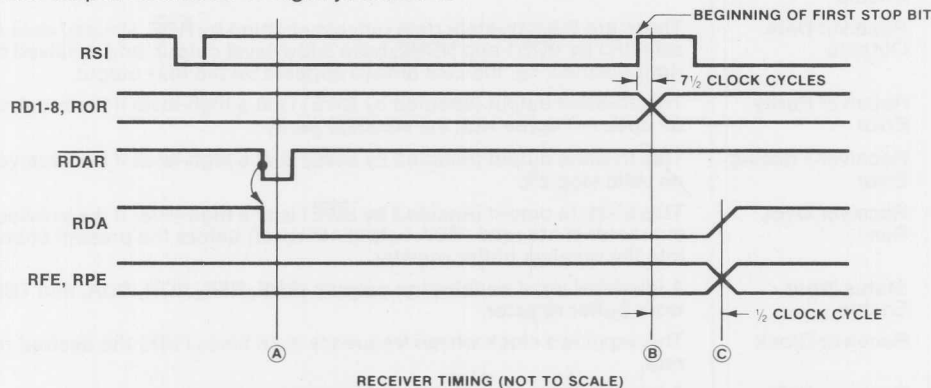
Description of Pin Functions

Pin No.	Symbol	Name	Function															
1	V _{cc}	Power Supply	+ 5 volt Supply															
2	NC		No connection															
3	GND	Ground	Ground															
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8-RD1) of the receiver buffer register.															
5-12	RD8-RD1	Receiver Data Outputs	These are the 8 tri-state data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.															
13	RPE	Receiver Parity Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.															
14	RFE	Receiver Framing Error	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.															
15	ROR	Receiver Over Run	This tri-state output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.															
16	$\overline{SWE}$	Status Word Enable	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.															
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.															
18	$\overline{RDAR}$	Receiver Data Available Reset	A low-level input resets the RDA output to a low-level.															
19	RDA	Receiver Data Available	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.															
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.															
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.															
22	TBMT	Transmitter Buffer Empty	This tri-state output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register may be loaded with new data.															
23	$\overline{TDS}$	Transmitter Data Strobe	A low-level input strobe enters the data bits into the transmitter buffer register.															
24	TEOC	Transmitter End of Character	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one-half of a TCP period in the case of continuous transmission.															
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.															
26-33	TD1-TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines, as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.															
34	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.															
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE.															
36	NSB	Number of Stop Bits	This input selects the number of stop bits. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits. Selection of two stop bits when programming a 5 data bit word generates 1.5 stop bits.															
37-38	NDB2, NDB1	Number of Data Bits/Character	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: <table><tr><td>NDB2</td><td>NDB1</td><td>data bits/character</td></tr><tr><td>L</td><td>L</td><td>5</td></tr><tr><td>L</td><td>H</td><td>6</td></tr><tr><td>H</td><td>L</td><td>7</td></tr><tr><td>H</td><td>H</td><td>8</td></tr></table>	NDB2	NDB1	data bits/character	L	L	5	L	H	6	H	L	7	H	H	8
NDB2	NDB1	data bits/character																
L	L	5																
L	H	6																
H	L	7																
H	H	8																
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table: <table><tr><td>NPB</td><td>POE</td><td>MODE</td></tr><tr><td>L</td><td>L</td><td>odd parity</td></tr><tr><td>L</td><td>H</td><td>even parity</td></tr><tr><td>H</td><td>X</td><td>no parity</td></tr><tr><td></td><td></td><td>X = don't care</td></tr></table>	NPB	POE	MODE	L	L	odd parity	L	H	even parity	H	X	no parity			X = don't care
NPB	POE	MODE																
L	L	odd parity																
L	H	even parity																
H	X	no parity																
		X = don't care																
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.															

RECEIVER OPERATION

Data is received in serial form at the RSI input. When no data is being received the RSI input must remain high. The data is clocked through the RCP. The clock rate is 16 times the data rate. (A) A low level on RDAR clears the RDA line. (B) During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to

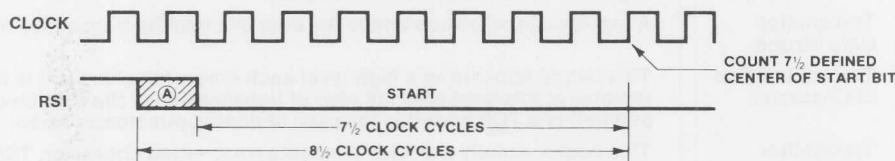
the least significant bit RD1. A logic high on ROR indicates overruns. An overrun occurs when RDA has not been cleared before the present character was transferred to the RBRegister. (C) $\frac{1}{2}$ clock cycle later RDA is reset to a logic high, RPE and RFE are evaluated. A logic high or RFE indicates an invalid stop bit was received, a framing error. A logic high on RPE indicates a parity error.



START BIT DETECTION

The receiver uses a 16X clock for timing. (A) The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count $7\frac{1}{2}$. If the receiver clock is a

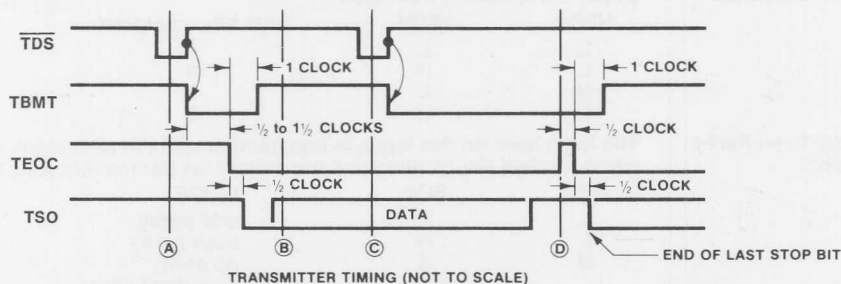
symmetrical square wave, the center of the start bit will be located within $\pm \frac{1}{2}$ clock cycle, $\pm \frac{1}{32}$ bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TSO. (A) Data is loaded into the transmitter buffer register from the inputs TD1 through TD8 by a logic low on the TDS input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TDS. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TD1. (B) The rising edge of TDS clears TBMT. $\frac{1}{2}$ to $1\frac{1}{2}$ clock cycles later data is transferred to the register and

TEOC is cleared. $\frac{1}{2}$ cycle later transmission starts. Output data is clocked by TCP. The clock rate is 16 times the data rate. $\frac{1}{2}$ clock cycle later TBMT is reset to a logic high. (C) A second pulse on TDS loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. (D) Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



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